REMARKS

Claims 1-10 and 12-27 are pending in this application.

Claim 10 has been amended to recite that the active element is "a high power" active element. Support for this amendment is found throughout the specification and claims as originally filed.

New claims 12-27 have been added to further define the present invention. Support for new claims 12-27 is found throughout the specification and claims as originally filed.

No new matter has been added.

In view of the amendment to claim 10, new claims 12-27, and the remarks set forth below, further and favorable consideration is respectfully requested.

I. Claims 1-8, as now amended, are rejected under 35 U.S.C. §103(a) as being unpatentable over Shibasaki et al. (U.S. Patent No. 5,430,310) in view of Ishikawa (U.S. Patent No. 6,294,446).

The Examiner states that it would have been obvious to the skilled artisan to form Shibasaki's device having the buffer layer which is a super lattice as taught by Ishikawa in order to reduce threading dislocations.

Applicant's note that the Examiner did not reject claim 10, but may have intended to reject claim 10. Please see page 4, paragraph 3, of the outstanding Office Action.

Claim 10 has been amended to recite a high power semiconductor device comprising an active layer having a high power active element.

New dependent claims 12-27 have been added to further define the invention, for example to require that the substrate be GaAs (claim 16), that the buffer layer be GaAs/AlGaAs super lattice (claims 12-14), that the active layer be doped (claim 15), and requiring undoped GaAs buffer layers (claim 13), etc.

Shibasaki discloses a FET including a GaAs or Si substrate having a buffer layer selected from AlGaAsSb, AlGaPSb, AlInAsSb and AlIbPSb provided thereon, and an InAs channel layer provided on the buffer layer, where the substrate has a lattice constant different from that of InAs.

Shibasaki ***requires*** that the buffer layer is a ***simple*** structure, in order to ensure ease of production, reliability of the resulting device, and to ensure thermal stability and freedom from property changes over time, of the device. See col. 6, lines 3-12, and lines26-33. Shibasaki teaches that the structure of the buffer layer can be simplified on the basis of the finding that the a layer like an AlGaAsSb layer, can absorb the stress generated by the lattice mismatching between the substrate and the InAs layer, and can form a smooth surface.

Shibasaki teaches in Example 1, a GaAs substrate having a resistivity of 10^7 Ω-cm or higher. Shibasaki does not teach a buffer layer that is a super lattice.

Ishikawa teaches a transistor with a T-shaped gate electrode including a GaAs substrate, and ***requiring*** a super-lattice buffer layer, and an InGaAs channel layer disposed between upper and lower AlGaAs gap layers.

New dependent claims 12-27 have been added to further define the invention, for example to require that the substrate be GaAs, that the buffer layer be GaAs/AlGaAs super lattice, that the active layer be doped, and requiring undoped GaAs buffer layers.

Authority regarding Prima Facie Obviousness:

MPEP 2143 discusses the requirements of a *prima facie* case of obviousness. First there must be some suggestion or motivation to combine the reference teachings or to modify the reference, and second there must be a reasonable expectation of success. Finally, the prior art reference or references when properly combined, must teach or suggest all the claim limitations.

MPEP 2143.01 states that there are three possible sources for a motivation to combine references: the nature of the problem being solved, the teachings of the prior art, and the knowledge of one of ordinary skill in the art. Further, MPEP 2145 (X)(D)(2) states that "It is improper to combine references where the references teach away from their combination."

This section quotes *In re Grasselli*, 713 F.2d 731 (Fed. Cir. 1983) which court held that a claimed catalyst which contained both iron and an alkali metal was not suggested by the combination of a reference which taught the interchangeability of antimony and alkali metal with the same beneficial result, combined with a reference expressly excluding antimony from , and adding iron to, a catalyst.

A combination of references may teach every element of a claimed invention, but without a motivation to combine the references, a rejection based on a *prima facie* case of obvious was held improper. *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998).

Further, where the prior art conflicts, all teachings must be considered. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. MPEP 2143.01 further states that a proposed modification cannot render the prior art unsatisfactory for its intended purpose. If it does, then there is no suggestion or motivation to make the proposed

modification. Further, the proposed modification cannot change the principle operation of a reference. MPEP 2141.02 states that prior art must be considered in its entirety, including disclosures that teach away from the claims. See also MPEP 2145 (X)(D).

Motivation to Combine:

It is submitted that a case of *prima facie* obviousness has not been established, because the combination of Shibasaki and Ishikawa, is improper. The combination of Shibasaki and Ishikawa is improper because there is no suggestion or motivation supporting the combination. Specifically, Shibasaki ***requires*** a simple buffer layer while Ishikawa ***requires*** a super-lattice buffer layer. Accordingly, the skilled artisan in view of Shibasaki ***requiring*** a simple buffer layer, would have no motivation to look to art requiring a super-lattice buffer layer, i.e., Ishikawa. Likewise, the skilled artisan in view of Ishikawa requiring a super-lattice buffer layer, would have no motivation to look to art ***requiring*** a simple buffer layer, i.e., Shibasaki.

Further, because Shibasaki ***requires*** a simple buffer layer, Shibasaki ***teaches away*** from any layer that is not a simple buffer layer, i.e., Shibasaki ***teaches away*** from the super-lattice buffer layer of Ishikawa. Likewise, because Ishikawa ***requires*** a super-lattice buffer layer, Ishikawa ***teaches away*** from any layer that is not a super-lattice buffer layer, i.e., Ishikawa ***teaches away*** from the simple buffer layer of Shibasaki. Thus, Shibasaki and Ishikawa, ***teach away from each other.*** Please see MPEP 2145 (X)(D)(2), discussed above.

Motivation to Modify Properly Combined References:

It is submitted that even if the combination of Shibasaki and Ishikawa were proper, there is no motivation to modify Shibasaki by substituting the super-lattice buffer layer of Ishikawa for the simple buffer layer of Shibasaki. There is no motivation to modify the device of Shibasaki because Shibasaki ***requires a buffer layer that is a simple structure***. Again, Shibasaki and Ishikawa, ***teach away*** from each other. Please see MPEP 2143.01.

Shibasaki discloses a FET including a semiconductor substrate 1, a first compound semiconductor layer (buffer layer) 2, an InAs layer (channel layer) 3, and a second compound semiconductor layer 4. Shibasaki requires that the substrate 1 have a lattice constant different from that of the InAs channel layer 3.

Shibasaki states that in order to obtain a high quality InAs film, the buffer layer formed between the substrate and the InAs film must have certain characteristics. In particular, Shibasaki states that the buffer layer should: ensure substantial lattice matching with the InAs layer; have band gaps greater than that of the InAs layer; have a smooth surface free of defects; have a ***simple structure*** to be thermally stable and free of property changes with time; prevent the occurrence of any substrate leakage current at the interface between the InAs layer and the buffer layer; have a structure having only a low parasitic capacitance; be an electric insulator. See Shibasaki, abstract thereof, as well as col. 5, line 64 to col. 6, line 21, and col. 10, lines 8-22. Shibasaki also states that four kinds of compound semiconductors, AlGaAsSb, AlInAsSb, AlInPSb and AlGaPSb, can satisfy the above requirements if the compositional ratios thereof are properly selected. According to Shibasaki, there are three methods for determining the range of acceptable compositional

parameters, which methods are described in detain at col. 10, line 58 to col. 13, line 36.

In view of the foregoing, it is clear that the buffer layer of Shibasaki **requires certain specific characteristics** in order for the Shibasaki FET device to **function in its intended manner.**

The Examiner contends that it would have been obvious to substitute the super lattice buffer layer of Ishikawa for the buffer layer of Shibasaki in order to "reduce threading dislocations."

However, in view of the specific requirements of the Shibasaki buffer layer, as noted above, substituting the Ishikawa super lattice buffer layer for the buffer layer used in the Shibasaki device falls short of what is required of the buffer layer specified in the Shibasaki reference. Please see MPEP 2143.01.

The Examiner has not identified how the Ishikawa super lattice buffer layer would meet the specific requirements of the simple buffer layer of Shibasaki. The highly specific requirements of the Shibasaki buffer layer, and the detailed methods set forth in Shibasaki to determine whether a compound semiconductor is suitable to function as a buffer layer in the Shibasaki device, demonstrate ***no motivation*** to substitute the Ishikawa super lattice buffer layer for the Shibasaki buffer layer.

In addition, even if one were motivated to substituted the Ishikawa super lattice buffer layer for the Shibasaki buffer layer, undue experimentation would be required to determine its suitability as a buffer layer in the Shibasaki device.

One particular specific requirement of the Shibasaki device, as noted in the abstract, as well as at col. 6, lines 3-33, and col. 17, lines 16-18, is that the buffer layer can be simplified on the basis of the finding that the buffer layer, like an AlGaAsSb layer, can absorb the stress generated by the

lattice mismatching between the substrate and the InAs layer, and can form a smooth surface.

The super lattice buffer layer of Ishikawa does not have a simple structure, much less a simple structure embodying the other requirements of the Shibasaki buffer layer. As is stated in Shibasaki, the buffer layer needs to be a simple structure because a simple structure buffer layer ensures ease of production and reliability of the resultant device, and ensures thermal stability and freedom from property changes over time. Shibasaki, col. 6, lines 6-12.

Accordingly, one of ordinary skill in the art would not be motivated to replace the Shibasaki buffer layer with the Ishikawa buffer layer, as the super lattice buffer layer of Ishikawa, which does not have a simple structure, would negatively affect the production and reliability of the Shibasaki device, and/or the stability of the thermal characteristics and properties of the Shibasaki device, thus rendering the Shibasaki device unsatisfactory for its intended purposes. Again, MPEP 2143.01 states that a proposed modification cannot render the prior art unsatisfactory for its intended purpose. If it does, then there is no suggestion or motivation to make the proposed modification

Further, assuming *arguendo* motivation to modify Shibasaki existed, none of the presently cited references (Shibasaki and Ishikawa), taken alone or together, disclose, teach or suggest a high power semiconductor device including an active layer having a high power active element formed therein, as required by independent claims 1 and 10. Present claims 2- 8 are directly or indirectly dependent on claim 1.

In view of the foregoing, it is submitted that Examiner has not established a case of *prima facie* obviousness, because the combination of Shibasaki and Ishikawa is improper. Assuming *arguendo* the combination proper, it is submitted that nothing in Shibasaki and Ishikawa, taken alone

or together, render the claimed invention obvious within the meaning of 35 USC § 103. Accordingly, the Examiner is respectfully requested to withdraw this rejection.

II. Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Shibasaki et al. (U.S. Patent No. 5,430,310) in view of Ishikawa (U.S. Patent No. 6,294,446) and further in view of Usagawa et al. (U.S. Patent No. 5,373,191).

The Examiner states that it would have been obvious to the skilled artisan to form the Shibasaki and Ishikawa device having the active layer as taught by Usagawa including an n-type collector layer, a p-type base layer and an n-type emitter layer, in order to form a bipolar transistor.

Usagawa teaches at col. 10, embodiment 6, a base electrode including a GaAs substrate, an n+GaAs layer with Si, a n-GaAs layer with Si, a p-GaAs base layer with Be, an n-AlGaAs layer with Si, and an n-GaAs layer with Si.

Present claim 9 is dependent on claim 1, and requires a collector layer of a first conducting type, a base layer of a second conducting type and an emitter layer of the first conducting type, where the base layer of a second conducting type is formed on the collector layer, and where an emitter layer of the first conducting type is formed on the base layer.

It is again submitted that a case of *prima facie* obviousness has not been established, because the combination of Shibasaki and Ishikawa, is improper. Further, assuming *arguendo* the combination proper, there is no motivation to modify Shibasaki by replacing the required simple buffer layer with the super-lattice layer required by Ishikawa. Please see the above discussion presented responsive to the rejection of claim 1-8 as obvious over Shibasaki in view of Ishikawa.

Usagawa does not provide the necessary motivation to combine Shibasaki and Ishikawa.

Assuming *arguendo* the combination proper, none of Shibasaki, Ishikawa, and/or Usagawa, teach or suggest the present invention.

More specifically, none of the presently cited references (Shibasaki, Ishikawa, Usagawa), taken alone or together, disclose, teach or suggest a high power semiconductor device including an active layer having a high power active element formed therein, as is recited in independent claim 1. Present claim 9 is dependent on claim 1.

Although Shibasaki relates to a FET that may transit and receive high frequency radio waves (col. 2, lines 51-59), no where is it stated in Shibasaki that the device is a ***high power device***. As was noted in Applicants Reply to the Office Action dated June 30, 2003, the specification at page 11, lines 29-31, or page 12, lines 13-15, clearly indicates that the devices of applicants claimed invention function under high power conditions. As an example of this distinction, whereas in an exemplary embodiment of the presently claimed invention, the device has a drain-source voltage of about 16 volts. See Applicant's Specification, page 8, lines 27-37, and Fig. 5.

As was noted in applicants Reply to the Office Action dated June 30, 2003, Ishikawa and Usagawa both fail to disclose "a high power semiconductor device" comprising "a high power active element", as presently required. The Examiner's attention is directed to applicants Reply to the Office Action dated June 30, 2003, which further distinguishes the presently claimed invention from Ishikawa and Usagawa.

In view of the foregoing, it is submitted that Examiner has not established a case of *prima facie* obviousness, because the combination of Shibasaki and Ishikawa is improper. Assuming

arguendo the combination proper, it is submitted that nothing in Shibasaki, Ishikawa and Usagawa, taken alone or together, render the claimed invention obvious within the meaning of 35 USC § 103. Accordingly, the Examiner is respectfully requested to withdraw this rejection.

Claim 10 has been amended to recite a high power semiconductor device comprising an active layer having a high power active element.

As noted above, none of the presently cited references (Shibasaki, Ishikawa, Usagawa) discloses, teaches or suggests a high power semiconductor device comprising an active layer having a high power active element formed therein, as is recited in currently amended independent claim 10.

In view of the foregoing, it is respectfully submitted that the presently claimed invention is patentable over the combination advanced by the Examiner, and it is respectfully requested that the rejection be withdrawn.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Amendment Transmittal (1)

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